



Thesis Project: *Optimized Emulation of IoT Devices*

Description of the units:

The Networked Embedded Systems (NES) group at RISE SICS is a part of the Computer Systems Laboratory. The current research focus is on wireless sensor networks and the Internet of Things. Among the group's key technologies are the Contiki operating system, uIP stack, COOJA/MSPSim, ContikiRPL and the IoT cloud service SICSthSense. The NES group conducts projects together with industry and academic partners from Sweden and across the world.

Thesis description:

As the Internet of Things (IoT) is rapidly moving from the research stage to commercialization, the tools for evaluating and testing devices, protocols, and software is becoming more and more important. COOJA/MSPSim is an IoT network simulator with support for emulation of individual devices. Originally developed at SICS, it is the primary tool to conduct tests and simulation experiments in the Contiki operating system community.

In this Master's thesis project, the objective is to *improve the performance of the MSPSim emulator through novel optimization techniques*. These improvements are focused on emulation speed to ensure that COOJA can simulate larger IoT networks than it can today. Simulating faster is important because COOJA is used for research and testing of Contiki software and other types of software. A slow simulation speed entails that fewer or smaller experiments have to be made in research projects, thereby reducing the quality of the research.

To mitigate such problems, one of the main technical goals with the project is to make MSPSim avoid the emulation of busy-looping until a certain condition occurs, and instead replace the busy-loop emulation with timers that wait for the condition. This replacement requires that the student develops a method to identify (1) that a busy-loop is being emulated, (2) any possible time constraints in the loop, and (3) which condition is being checked. Other possible paths of investigation is to provide a statistical overview of how much time of the total system lifetime that is spent busy-looping, identify busy-loops in the source code of the emulated firmware, and programming abstractions that replace Contiki's busy-looping code in an elegant manner. In case of a highly successful project, the student's work may be developed into an academic paper.

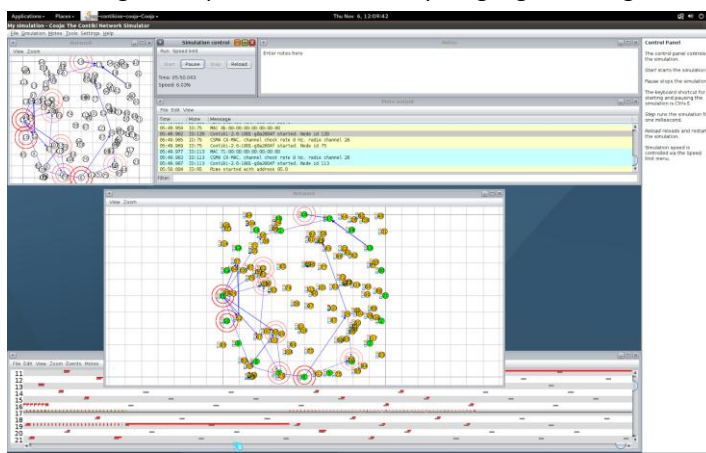
SICS will provide both background information and all the source needed to start on thesis project. The tasks of the Master's student for this thesis are:

- Study different approaches to improve emulation speed of the IoT device emulator MSPSim.
- Evaluate what parts of the code in typical embedded IoT software consumes most simulation time (Contiki OS software).
- Implement and evaluate relevant parts of the speed improvements in MSPSim.
- Investigate into ways to optimize the IoT applications and OS to speed up simulation.
- Document the work and the results in a Master's thesis.

Competence:

We are looking for a bright MSc student who has fulfilled the course requirements. Very strong skills in Java and C programming are required, as is good spoken and written English. Experience in assembly language is of high value.

Applications should include a brief personal letter, CV, and university grades. In your application, make sure to give examples of previous projects involving programming that you consider relevant for the position. Candidates are encouraged to submit their application as soon as possible. Suitable applicants will be interviewed as applications are received.



Start time: As soon as possible.

Duration: 20 weeks (30 hp.)

Location: RISE SICS, Kista, Sweden.

Contact person:

Joakim Eriksson, Ph.Lic & Senior Researcher, SICS

E-mail: joakime@sics.se

Nicolas Tsiftes, Ph.D & Senior Researcher, SICS

E-mail: nvt@sics.se

RISE SICS AB

Networked Embedded Systems Group,

Electrum Building,

Isafjordsgatan 22

SE-164 40 Kista, Stockholm