Optimal Register Allocation and Instruction Scheduling for LLVM

Roberto Castañeda Lozano – SICS, KTH

joint work with:

G. Hjort Blindell – KTH, SICS

M. Carlsson – SICS

F. Drejhammar – SICS

C. Schulte – KTH, SICS

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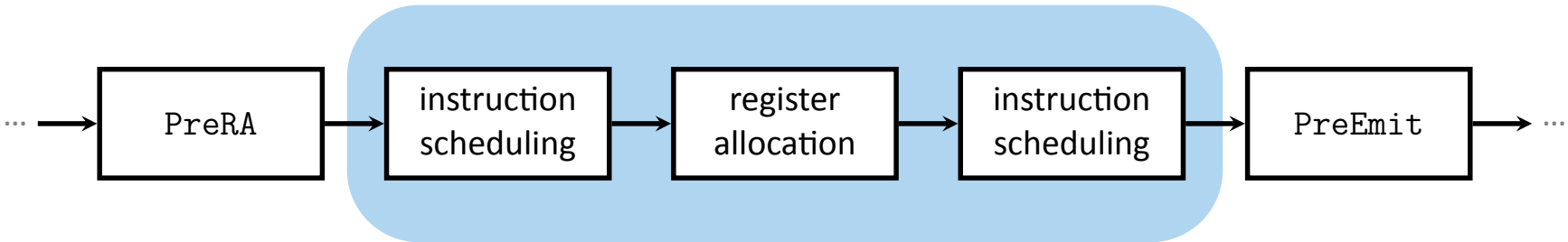
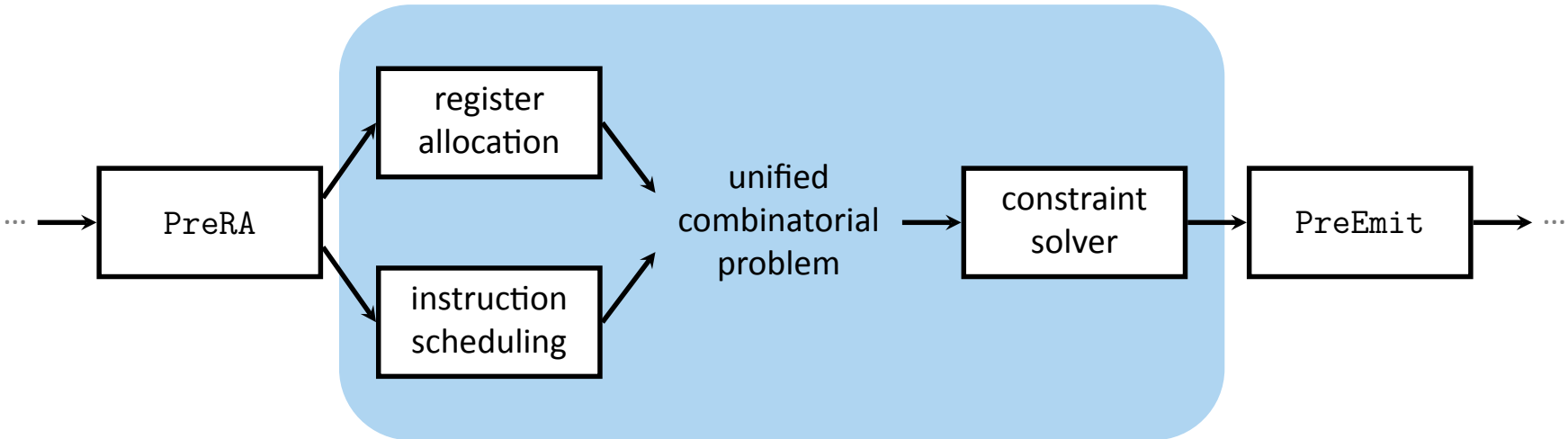
Code Generation in LLVM



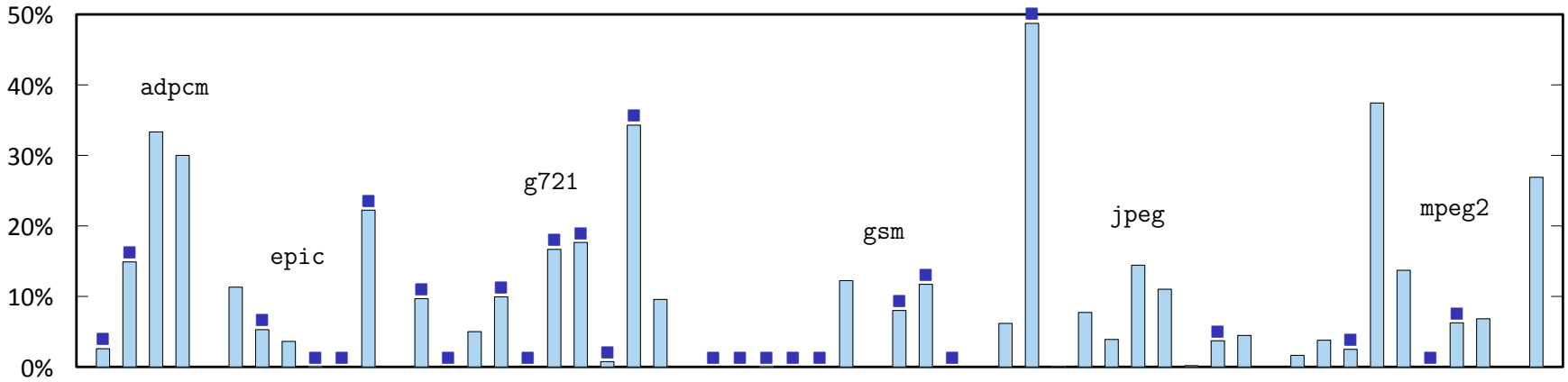
- Stages, heuristics
- Pros: compilation speed
- Cons: suboptimal, complex

Introducing Unison



- Integration, combinatorial optimization
- Pros: simple, optimal
- Cons: compilation slowdown

Speedup over LLVM 3.8



- 50 MediaBench functions
- Hexagon V4 processor
- Provably optimal (■) for 54% of the functions
- Compilation time: from seconds to minutes

Unison Is Practical and Effective

- Integrated
  - register allocation
  - instruction scheduling
- Simple, optimal, slower
- Complements LLVM:
  - traditional LLVM for compile/debug cycle
  - LLVM + Unison for release builds
- Useful analysis tool for LLVM developers
  - how good is my heuristic?